What is Claimed is:

[c1] A pair of programmable memory cells comprising a shared control gate, first and second floating gates having respective gate regions located on respective sides of the control gate, and dielectric structures located between said control gate and respective ones of said gates of said floating gates, wherein said control gate and said gates of said first and second floating gates are located within a space of a single lithographic square.

[c2] The pair of programmable memory cells of Claim 1 wherein respective heights of said control gate and said gates of said first and said second floating gate devices are optimize to achieve capacitance coupling therebetween.

[c3] The pair of programmable memory cells of Claim 1 further comprising a first bitline and a second bitline, wherein said first bitline is borderless to said first floating gate and said second bitline is borderless to said second floating gate.

[c4] The pair of programmable memory cells of Claim 1 further comprising a wordline interconnected to said control gate.

[c5] The pair of programmable memory cells of Claim 1 further comprising shallow trench isolation regions, said shallow trench isolation regions being located adjacent to said pair of memory cells.

[c6] The pair of programmable memory cells of Claim 5 wherein said shallow trench isolation regions are formed self-aligned to bitline diffusion regions that abut said pair of memory cells and edges of said first and second floating gates.

[c7] The pair of programmable memory cells of Claim 1 further comprising a common reference line that is located beneath an insulated portion of said control gate.

[c8] The pair of programmable memory cells of Claim 1 wherein said cells are EEPROM memory cells, non-volatile memory cells or flash memory cells.

[c9] The pair of programmable memory cells of Claim 5 further comprising patterned bitlines formed above said shallow trench isolation regions.

[c10] A pair of programmable memory cells comprising a single control gate, a first floating gate, a second floating gate, a first bitline, and a second bitline, wherein said control gate

is self-aligned to said first and second floating gates.

[c11] The pair of programmable memory cells of Claim 10 wherein said first bitline is borderless to said first floating gate and said second bitline is borderless to said second floating gate.

[c12] The pair of programmable memory cells of Claim 10 further comprising a wordline connected to said control gate, wherein said first bitline and said second bitline are both borderless to said control gate and said wordline.

[c13] The pair of programmable memory cells of Claim 10 wherein coupling between said floating gates and said control gate is controllable by heights of said floating gates.

[c14] The pair of programmable memory cells of Claim 10 further comprising shallow trench isolation regions, said shallow trench isolation regions being located adjacent to said pair of programmable memory cells.

[c15] The pair of programmable memory cells of Claim 14 wherein said shallow trench isolation regions are formed self-aligned to bitline diffusion regions that abut said pair of memory cells and edges of said first and second floating gates.

[c16] The pair of programmable memory cells of Claim 10 further comprising a common reference line that is located beneath an insulated portion of said control gate.

[c17] The pair of programmable memory cells of Claim 10 wherein said cells are EEPROM memory cells, non-volatile memory cells or flash memory cells.

[c18] A layout for a non-volatile memory cell comprising a programmable memory cell wordline borderless to a bitline.

[c19] The layout of Claim 18 wherein said wordline lies orthogonal to said bitline.